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(54) **SEMICONDUCTOR PACKAGE AND METHOD THEREFOR**

(71) Applicant: **Amkor Technology, Inc.**, Chandler, AZ (US)

(72) Inventors: **Hyung Il Jeon**, Gyeonggi-do (KR); **Ji Young Chung**, Gyeonggi-do (KR); **Byong Jin Kim**, Gyeonggi-do (KR); **In Bae Park**, Seoul (KR); **Jae Min Bae**, Seoul (KR); **No Sun Park**, Gyeonggi-do (KR)

(73) Assignee: **Amkor Technology, Inc.**, Tempe, AZ (US)

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CPC ***H01L 24/17*** (2013.01); ***H01L 23/49541*** (2013.01); ***H01L 23/49548*** (2013.01); ***H01L 23/49572*** (2013.01); ***H01L 24/81*** (2013.01)

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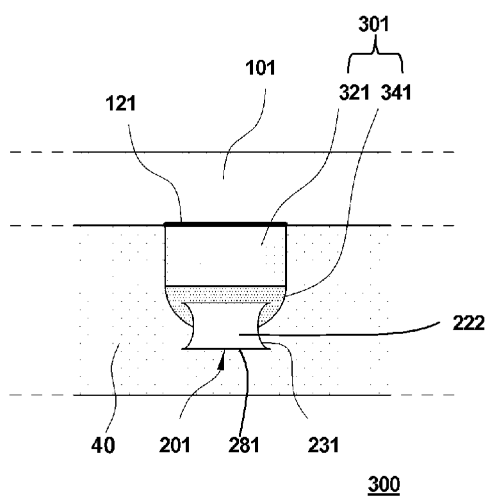
Primary Examiner — Roy Potter
(74) *Attorney, Agent, or Firm* — Kevin B. Jackson

(57) **ABSTRACT**

In one embodiment, an electronic package structure includes a lead having a first width. An electronic chip having a conductive bump on a major surface, the conductive bump has a second width greater than the first width. The conductive bump is attached to the lead such that a portion of the conductive bump extends to at least partially surround a side surface of the lead. A molding compound resin encapsulates the electronic chip, the conductive bump, and at least a portion of the lead. The lead is configured so strengthen the joining force between the lead and conductive bump.

20 Claims, 4 Drawing Sheets



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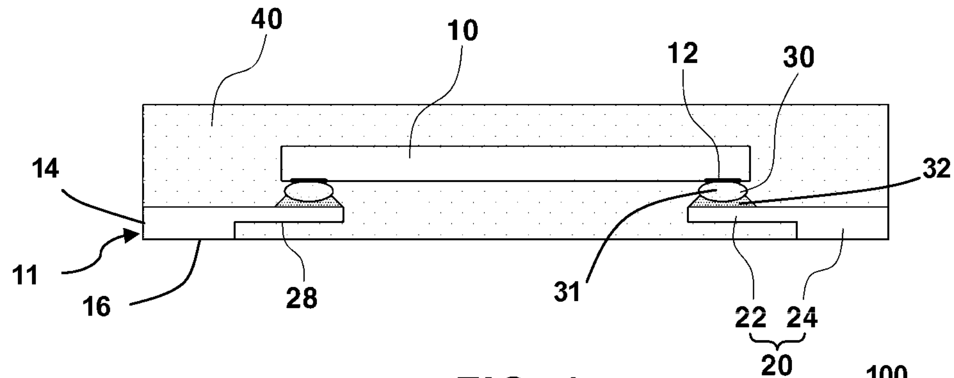


FIG. 1

100

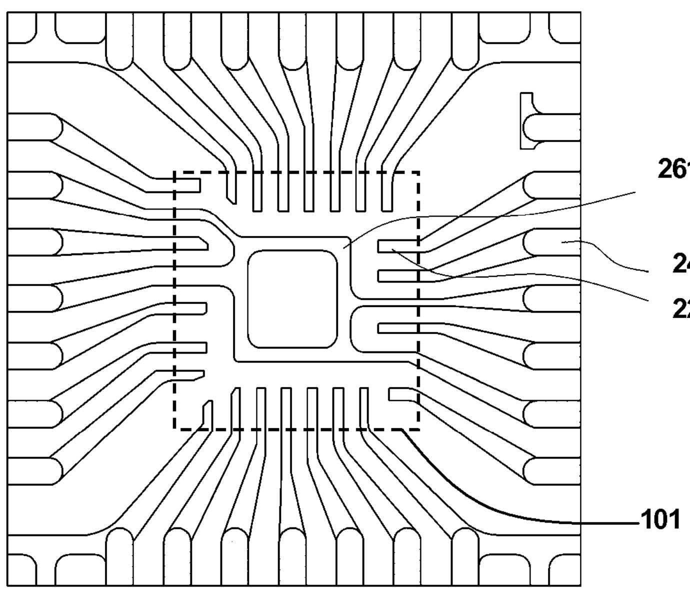


FIG. 2

200

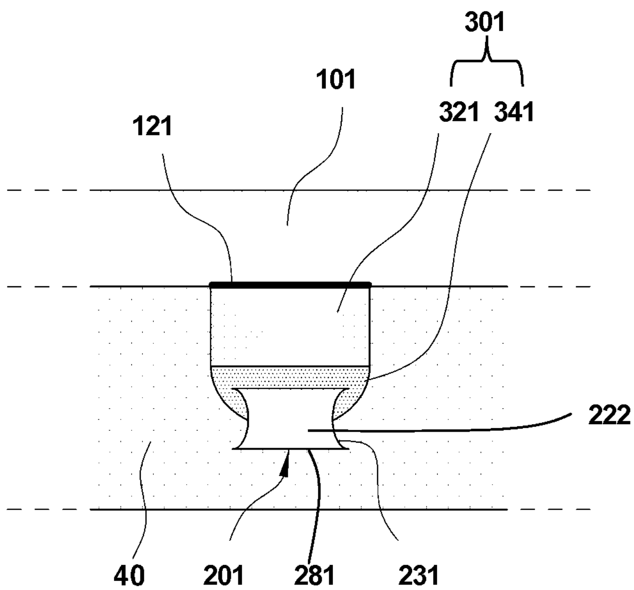


FIG. 3 300

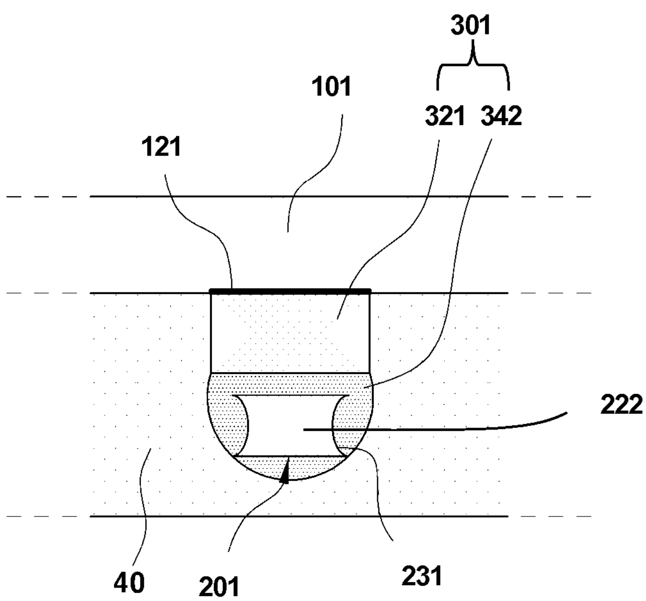


FIG. 4 400

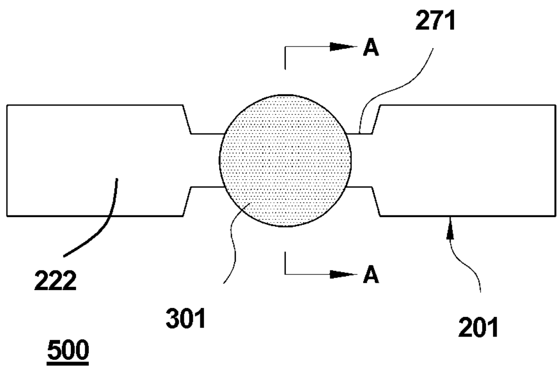


FIG. 5

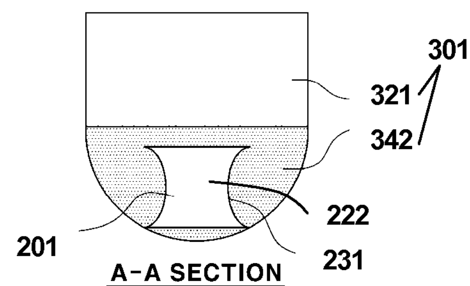


FIG. 5A

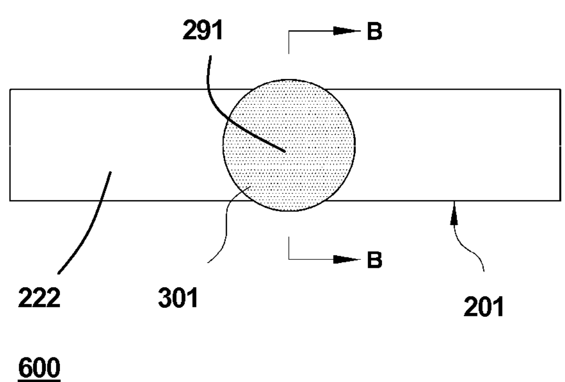


FIG. 6

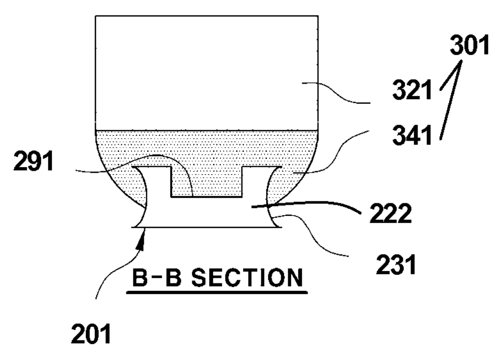
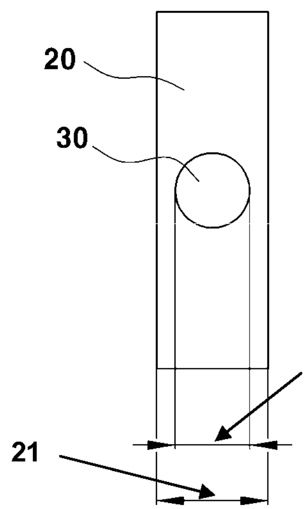


FIG. 6A



- RELATED ART -

FIG. 7A

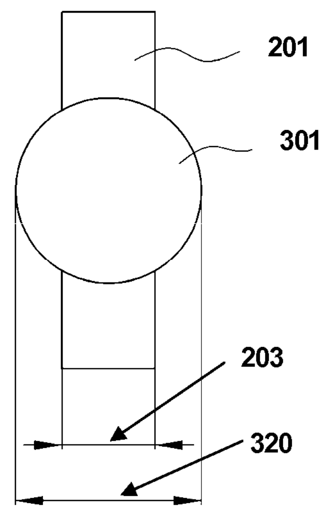


FIG. 7B

SEMICONDUCTOR PACKAGE AND METHOD THEREFOR

CROSS REFERENCE TO RELATED APPLICATION

This application claims priority to Korean Patent Application No. 10-2013-0126885 filed on Oct. 24, 2013, which is expressly incorporated by reference herein.

BACKGROUND

Embodiments disclosed herein relate generally to electronic packages, and, more particularly, to a semiconductor package in which a solder joint for joining a flip chip lead frame and an electronic device is improved in structure to have an enhanced coupling force and method of fabricating the same.

Generally, a conductive lead frame is a type of substrate used for fabricating a semiconductor package. The lead frame is the central supporting structure of such a package, and typically is fabricated by chemically etching or mechanically stamping a metal strip. The lead frame typically includes a side frame defining an entire framework, a chip pad for mounting one or more semiconductor chips, one or more tie bars integrally connecting the side frame to the chip pad, and a plurality of leads extending from the side frame in such a way as to be adjacent or proximate to all sides of the chip pad. A portion of the lead frame is internal to the package body or completely surrounded by a plastic encapsulant, such as a mold compound. Portions of the leads of the leadframe may extend externally from the package body or may be partially exposed therein for use in electrically connecting the package to another component. In certain semiconductor packages, a portion of the die pad of the leadframe also remains exposed within the package body.

There is a class of semiconductor packages referred to as near chip scale packages (CSP) that include very thin, fine pitch, and small area lead frames that approximate the size of the semiconductor chip. Such packages include the MicroLeadFrame® (MLF) style of packages. These packages typically have package body sizes in the 1 mm to 13 mm range and package heights in the 0.3 mm to 2.1 mm range. In order to enhance unit productivity, near chip scale packages such as MLF style packages are assembled in a matrix of multiple leadframes and encapsulated in an overmolding process. The individual MLF structures are then separated into individual packages typically using a sawing process, which cuts through the mold compound and the lead frames.

In some applications, flip chip attachment of semiconductor chips to lead frames is continuing to grow compared semiconductor chips connected using conductive wires. The growth of flip chip attachment is being driven by, among other things, form factor and product performance. Types of semiconductor chips seeing growth in flip chip attachment include microprocessors, application specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), digital signal processors (DSPs), media products, and graphics chips, among others.

Earlier versions of flip chip attached semiconductor chips used evaporated bumps (e.g., C4 bumps) and electroplated bumps (e.g., high-Pb bumps). Currently, the industry is moving towards an expanded use of conductive pillar structures (e.g., copper pillar structures) particularly with smaller geometry process nodes. Copper pillar structures are preferred because, among other things, they are configured to

provide small form factors to support smaller die sizes, improved electrical performance, and greener (i.e., lead-free) manufacturing solutions.

Using conductive pillar structures with near chip scale packages, such as MLF style packages has presented several manufacturing problems. Specifically, with the industry requirement for lead frames to have very fine lead pitches, the width of each lead is being reduced. Also, in order to improve electrical performance, the size of the conductive bumps, such as copper pillars, is being increased. However, with the reduced lead widths the solder joint formed between the pillar and the lead has been found to be unsatisfactorily weak and a source of reliability problems.

Accordingly, it is desirable to have a semiconductor package structure and method that overcome the issues with related flip chip packages described previously, as well as others. It is also desirable to have a structure and method that is cost effective, easy to integrate into assembly process flows, and reliable.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a cross-sectional view of a flip chip electronic package structure;

FIG. **2** shows a lead frame structure for use in embodiments of the present invention;

FIG. **3** illustrates a partial cross-sectional view of an electronic package in accordance with an embodiment of the present invention;

FIG. **4** illustrates a partial cross-sectional view of an electronic package in accordance with an embodiment of the present invention;

FIG. **5** illustrates a partial top view of an electronic package lead structure in accordance with an embodiment of the present invention;

FIG. **5**A illustrates a cross-sectional view of the embodiment of FIG. **5**;

FIG. **6** illustrates a partial top view of an electronic package lead structure in accordance with a further embodiment of the present invention;

FIG. **6**A illustrates a cross-sectional view of the embodiment of FIG. **6**;

FIG. **7**A illustrates a top view of a lead structure and a pillar structure of a related electronic package; and

FIG. **7**B illustrates a top view of a lead structure and a pillar structure of an electronic package in accordance with another embodiment of the present invention.

For simplicity and clarity of the illustration, elements in the figures are not necessarily drawn to scale, and the same reference numbers in different figures can denote the same elements. The use of the word about, approximately or substantially means that a value of an element has a parameter that is expected to be close to a stated value or position. However, as is well known in the art there are always minor variances that prevent the values or positions from being exactly as stated. Additionally, descriptions and details of well-known steps and elements may be omitted for simplicity of the description.

DETAILED DESCRIPTION OF THE DRAWINGS

The aspects of the present invention and methods for achieving the aspects will be apparent by referring to the embodiments to be described herein with reference to the accompanying drawings. It is understood that the embodiments described herein are illustrative only and that the present invention is not limited thereto, but can be implemented in alternative forms. Also, it is understood that the features of the various embodiments described herein can be combined with each other, unless specifically noted otherwise.

In general, the present embodiments relate to a structure and method for providing a stronger joining force for the bonding joint between conductive leads within a lead frame and the solder of conductive bumps. This stronger joining force is provided even if the lead width is reduced to support finer pitch lead frames and even if the width of the conductive pillars is increased. In one embodiment, each lead is configured having a width smaller than the width of the conductive bump and further configured to facilitate the flow of solder from the conductive bump partially or completely around each lead to provide a strengthened solder joint. In one embodiment, the bond finger portion of each lead is configured to strengthen the solder joint. In another embodiment, the land portion of each lead is configured to strengthen the solder joint. In one embodiment, each lead is configured having concave sides surface portions to provide the strengthened solder joint. In another embodiment, each lead is provided with a narrow neck portion that provides the strengthened solder joint. In a further embodiment, each lead is configured with a dimple portion that provides the strengthened solder joint.

Hereinafter, a semiconductor package **100** using a lead frame **11**, such as micro lead frame, is described with reference to FIG. **1**. FIG. **1** shows a cross-sectional view of a flip chip attached electronic device after semiconductor package **100** has been separated using a singulation process. As shown in FIG. **1**, semiconductor package **100** includes an electronic device, such as a semiconductor chip **10** attached to leads **20** of a lead frame **11** (e.g., a micro lead frame) using a conductive bump **30**. In a typical structure, semiconductor chip **10** includes a plurality of conductive bond pads **12** formed on a major surface of semiconductor chip **10** and electrically connected to various circuit elements within semiconductor chip **10**. A passivation layer (not shown) is typically formed on bond pads **12** and has openings to expose portions of bond pads **12**. An under bump metal (UBM) layer (not shown) is typically provided on the exposed portions of bond pads **12** and typically includes titanium and/or titanium-nitride. In a conductive pillar process, such as a copper pillar process, a photo-imageable resist (either a dry film or a spin-on film) is used to define where the pillar structure will be plated, and then a solder layer or solder cap can be applied to the tip of each pillar structure through a paste process or an electroplating process. The resist layer is then stripped, excess material can be etched, and then the solder layer can be subjected to a reflow process.

If bonding pads **12** on semiconductor chip **10** and each lead **20** were connected to each other by conductive wires as in the related art, a height for forming a loop of the conductive wires is required, thus undesirably leading to an increase in the entire thickness of the semiconductor package. Unlike a conductive wire structure, semiconductor package **100** is configured such that bonding pads **12** on semiconductor chip **10** and each lead **20** are connected to each other using the flip chip configuration in such a way as to enable the electric signal interchange to and from semiconductor chip **10** and leads **20**. Thus, such a structure advantageously reduces the entire thickness of the semiconductor package and provides a lighter, thinner, smaller, and more compact product.

In one embodiment, each lead **20** of lead frame **11** is configured to function similar to a chip mounting board for mounting the semiconductor chip **10** thereon. In one embodiment, a ground pad is provided within a central portion proximate to an end portion of each lead **20**. Further, each lead **20** includes a bond finger **22** where the flip chip is attached and a land portion **24** where semiconductor package **100** is attached to a next level of assembly (e.g., a motherboard). Land portion **24** further provides for electrical communication between semiconductor chip **10** and other electronic devices. A recessed or etched portion **28**, which is reduced in thickness by, for example, etching, is formed on or extending inward from a lower surface of bond finger **22**.

Semiconductor chip **10** is attached to bond fingers **22** of leads **20**. Specifically, in one embodiment bonding pads **12** on semiconductor chip **10** are connected to the bond finger **22** of each lead **20** using a flip chip structure in such a way as to permit the electric signal interchange, and then a molding process is performed to seal the semiconductor chip **10**, the flip chip structure, and at least portions of leads **20** with a molding compound resin **40** to provide related semiconductor package **100** as shown in FIG. **1**.

Conductive bumps **30** include, for example, a copper pillar **31** and a solder portion or layer **32**. As described previously, copper pillars **31** can be formed overlying bond pads **12** using electroplating techniques or other techniques as known to those of ordinary skill in the art. Solder portion **32** can be integrally formed on an end of copper pillar **31** by plating or by depositing a solder paste. In one embodiment, an outer surface **14** and a lower surface **16** of the land portion **24** of each lead **20** are exposed to the outside, and recessed portion **28** of each lead **20** is filled with molding compound resin **40**, thus increasing a coupling force between each lead **20** and molding compound resin **40**.

In related packages, copper pillar **31** of conductive bump **30** has a typical width or diameter of 50 microns. Bond fingers **22** of leads **20** typically have widths of 70 microns. This size configuration provides a pillar-to-lead ratio of 0.7, which allows solder portion **32** formed on the end of copper pillar **31** to be electrically fused to and easily seated on the top surface of bond finger **22** of each lead **20**. However, if the width of each lead is reduced and the size of the conductive bump is increased to support the demand for fine pitch lead frames for each lead and the increase in size or width of the copper pillar portion of the conductive bump, the solder joint of the conductive bump relative to each lead has been found to be weakened. The following embodiments are configured to address, among other things, strengthening this solder joint.

FIG. **2** illustrates a top view of a lead frame **200** for use with the present embodiments. In one embodiment, lead frame **200** is configured, for example, as a micro lead frame and includes a plurality of leads **201**. Leads **201** of lead frame **200** are configured to function similar to a chip mounting board for mounting a semiconductor chip **101** thereon. In one embodiment, ground pad **261** is provided within a central portion proximate to an end portion of each lead **201**. In one embodiment, plurality of leads **201** can include at least four sets disposed proximate to four sides of ground pad **261**. Further, each lead **201** can include a bond finger **222** where electronic chip or semiconductor chip **101** is attached and a land portion **241** where the electronic package is attached to a next level of assembly (e.g., a motherboard). Land portion **241** further provides for electrical communication between semiconductor chip **101** mounted thereon and other electronic devices.

FIG. **3** illustrates a partial cross-sectional view of an electronic package **300**, such as a semiconductor package **300**, in accordance with a first embodiment including lead frame **200** illustrated in FIG. **2**. Semiconductor package **300** is illustrated with one lead from the plurality of leads **201**, which can be configured as a chip mounting pad or chip mounting board. In semiconductor package **300**, lead **201** can include a bond finger **222** and a land portion **241** (illustrated in FIG. **2**). In one embodiment, bond finger **222** can be formed in an inner region of lead **201** in a longitudinal direction thereof to serve as a place to which semiconductor chip **101** is flip chip attached. In one embodiment, land portion **241** can be formed in an outer region of each lead **201** to be electrically connected to a next level of assembly, such as a mother board and placed in electrical communication with other electronic devices. In some embodiments, an etched or recessed portion **281**, which is reduced in thickness by etching, can be formed on a lower surface of bond finger **222**.

Semiconductor chip **101** can be attached to or mounted to lead **201** using a conductive bump structure **301** or conductive bump **301**. In one embodiment, conductive bump structure **301** is connected to a bond pad **121** on a surface of semiconductor chip **101** and connected to bond finger **222** of lead **201**.

In accordance with the present embodiment, conductive bump structure **301** includes a conductive pillar **321** and a solder portion **341** or solder cap **341**. In some embodiments, conductive pillar **321** includes a metallic material, such as copper or other materials as known to those of ordinary skill in the art. In one embodiment, conductive pillar **321** can be formed using a photo-imageable layer and an electroplating process. Solder portion **341** can then formed on a tip or end portion of conductive pillar **321** using an electroplating process or a solder paste deposition process. In one embodiment, solder portion **341** can be a silver/tin solder or another alloy solder. After solder portion **341** is formed, the photo-imageable layer can be removed. In an optional step, solder portion **341** and conductive pillar **321** can be subjected to a reflow process. In one embodiment, semiconductor chip **101** with conductive bump structures **301** is placed using, for example, a pick and place tool into contact with plurality of leads **201**. The assembly is then subjected to an elevated temperature to reflow solder portion **341** to form a solder joint with lead **201**.

In accordance with the present embodiment and as illustrated in FIG. **7**B, which is a top view of lead **201** (i.e., the upper bonding surface), the width **203** of each lead **201** (i.e., the width proximate to the upper bonding surface of the lead) is reduced compared to related packages as illustrated in FIG. **7**A. In FIG. **7**A, related lead **20** has a width **21**, which is typically 70 microns or more. In one embodiment, the width **203** of each lead **201** is about 60 microns or less so as to support packages having finer lead pitches, such as micro lead frame packages. Further, in accordance with the present embodiment, conductive pillar **321** has a width **320** of about 120 microns or more so as to improve electrical performance of the packaged semiconductor device. In the related packages as illustrated in FIG. **7**A, the related bump **30** has a width **35**, which is typically 50 microns or less.

Stated another way, related devices typically have a bump-to-lead width ratio of about 0.7 or less whereas the present embodiment has a bump-to-lead width ratio of about 2 or more. In related devices, such a bump-to-lead width ratio would lead to weakened solder joints between the conductive bump and the leads as described previously. In accordance with the present embodiment, the semiconductor package **301** is configured to provide an enhanced solder joint or a stronger joining force for the joint between each lead **201** and solder portion **341** of conductive bump **301**. More particularly, lead **201** is configured so that solder portion **341** at least partially surrounds the outer surface area of each lead **201**. In one embodiment, solder portion **341** extends beyond the top surface of each lead **221** and attaches to at least portions of side surfaces of each lead **201** as generally illustrated in FIG. **3**. In accordance with the present embodiment, even if the width of the lead **201** is reduced and the size of the copper pillar **321** is increased in this manner, it is possible to significantly strengthen a joining force for a joint between each lead **201** and solder portion **341** of conductive bump **301**.

In some embodiments, each lead **201** is provided with a bond finger portion **222** configured to facilitate the flow of solder portion **341** around at least portions of the side surfaces of each lead **201**. In a preferred embodiment, the side surfaces of each lead can be provided with a generally curved shape or concave portion **231** to further strengthen the joining force between bond finger **222** of each lead **201** and solder portion **341** of conductive bump **301** by filling at least portions of concave portions **231** with parts of solder portion **341**. Concave portions **231** are configured to increase the surface area of the bonding surface for forming the solder joint with solder portion **341**.

After the attachment process, at least portions of semiconductor chip **101**, portions of each lead **201** and conductive bumps **301** are covered or encapsulated with molding compound resin **40** or encapsulating layer **40**. In one embodiment, molding compound resin **40** can be formed using an overmolding process. After the overmolding process, the semiconductor packages can be separated into individual components using a singulation process, such as a sawing process. Portions of leads **201** and/or lead frame **200** (e.g., ground pad **261**) can be exposed to the outside through molding compound resin.

FIG. **4** illustrates a partial cross-sectional view of an electronic package **400**, such as a semiconductor package **400**, in accordance with a second embodiment. Semiconductor package **400** is similar to semiconductor package **300** except solder layer **342** in semiconductor package **400** extends all the way around or entirely surrounds a portion of bond finger **222** of lead **201** thus further enhancing or strengthening the joining force for the joint (i.e., solder joint) between each lead **201** and solder layer **342** of conductive bump **301**. Even if the width of the lead **201** is reduced and the size of the copper pillar **321** is increased as illustrated in FIG. **7**B, the present embodiment is configured to strengthen the joining force for a joint between each lead **201** and solder layer **342** of conductive bump **301**.

FIG. **5** illustrates a partial top of an electronic package lead structure **500** in accordance with a third embodiment. FIG. **5**A illustrates a cross-sectional view of lead structure **500** taken along reference line A-A in FIG. **5**. In order to strengthen the joining force for the joint between the bond finger **222** of each lead **201** and the solder portion **341** of conductive bump **301**, a portion of the bond finger **222** where solder layer **34** is to be fused is configured to have a narrow neck portion **271**, which has a width smaller than an original width of the bond finger **222**. Other portions of bond finger **222** can be of the original width to provide additional strength and/or stability to the structure. In one embodiment, narrow neck portion **271** is formed using masking and etching techniques.

In accordance with the present embodiment, when solder portion **342** formed on the end of copper pillar **321** of conductive bump **301** is soldered onto the upper surface of bond finger **222** of lead **201**, solder portion **342** partially or completely surrounds the surface area of bond finger **222**, and narrow neck **271** is formed on bond finger **222** of each lead **201**. In this configuration solder portion **342** can more easily surround the surface area of a portion of bond finger **222**, thus resulting in strengthening the joining force for the joint between bond finger **222** of each lead **201** and solder portion **342** of conductive bump **301**. In one embodiment, lead structure **500** can include concave portions **231** along or in the side surfaces of neck portion **271**.

FIG. **6** illustrates a partial top of an electronic package lead structure **600** in accordance with another embodiment. FIG. **6**A illustrates a cross-sectional view of lead structure **600** taken along reference line B-B in FIG. **6**. In order to strengthen the joining force for the joint between bond finger **222** of each lead **201** and solder portion **341** of the conductive bump **301**, one or more dimples **291** can be formed on a major surface (e.g., the upper surface) of bond finger **222** onto which solder portion **341** is fused. In one embodiment, dimple **291** can be formed using a masking and etching process. In another embodiment, dimple **291** can be formed using stamping techniques. In an alternative embodiment dimple **291** can be formed in the lower surface of bond finger **222** when solder portion **341** completely surrounds a portion lead **201**. In another embodiment, dimples **291** can be formed on both surfaces.

In accordance with the present embodiment, when solder portion **341** formed on the end of copper pillar **321** of conductive bump **301** is soldered onto the upper surface of bond finger **222** of lead **201**, solder portion **341** partially or completely surrounds the surface area of the bond finger **222**. In addition, dimple **291** is formed on bond finger **222** of each lead **201**. In this configuration of bond finger **222**, solder portion **341** can more easily surround the surface area of the bond finger **222** while filling dimple **291**, thus resulting in strengthening the joining force for the joint between bond finger **222** of each lead **201** and solder portion **341** of conductive bump **301**. Dimple **291** is configured to increase the surface area for forming the solder joint with solder portion **341**. In one embodiment, lead structure **600** can include concave portions **231** along or in the side surfaces of bond finger **222**. In one embodiment, dimple **291** is between a concave portions **231** as generally illustrated, for example, in FIG. **6**A.

Those skilled in the art will appreciate that the described embodiments can also be implemented on land portions **241** of each lead **201** as well as bond fingers **222**. By way of example, in land portion implementations, solder portion **341** preferably only partially surrounds the surface area of the land portions and such land portions can be configured to include one or more concave portions **231** to further enhance the strength of the bonding force between solder portion **341** and each lead **201**.

From all of the foregoing, one skilled in the art can determine that according to one embodiment, a semiconductor package includes a semiconductor chip, a plurality of leads on which the semiconductor chip is mounted, a conductive bump electrically connecting a bonding pad of the semiconductor chip with a bond finger of each of the leads, and molding compound resin molded to seal the semiconductor chip, the leads, and the conductive bump. A size of a conductive pillar of the conductive bump is larger than a width of each of the leads, so that a solder is soldered while partially or completely surrounding a surface area of the bond finger, when the solder formed on an end of the conductive pillar is soldered onto an upper surface of the bond finger of the lead.

In another embodiment, a concave portion may be formed on each of opposite sides of the bond finger by an etching process. In a further embodiment, a portion of the bond finger onto which the solder is fused may undergo the etching process to form a narrow neck, which has a width smaller than an original width of the bond finger. In a still further embodiment, a dimple may be formed on the upper surface of the bond finger onto which the solder is fused.

From all of the foregoing, one skilled in the art can determine that according to another embodiment, a semiconductor package (for example, element **300**, **400**, **500**, **600**) comprises a plurality of leads (for example, element **201**), each lead having a bond finger (for example, element **222**). A semiconductor chip (for example, element **101**) having a plurality of conductive bumps (for example, element **301**), each conductive bump including a conductive pillar (for example, element **321**) and a solder portion (for example, **341**, **342**), each conductive bump attached to one of the bond fingers. A molding compound resin (for example, element **40**) is molded to seal the semiconductor chip, at least portions of the leads, and the conductive bump, wherein a width (for example, element **320**) of the conductive pillar is larger than a width (for example, element **203**) of each of the leads, and wherein the solder portion extends beyond an upper surface of the bond finger and at least partially surrounds a surface area of a portion of the bond finger.

In another embodiment, the solder portion (for example, element **342**) completely surrounds the surface area of the portion of the bond finger. In a further embodiment, at least a portion of the surface area comprises a concave portion (for example, element **231**). In a still further embodiment, each bond finger has concave portions (for example, element **231**) on opposing side surfaces in cross-sectional view. In another embodiment, the semiconductor package can further comprise a dimple (for example, element **291**) in a major surface of the bond finger, wherein the dimple is disposed between the concave portions. In a further embodiment, a portion of the bond finger where the conductive bump is attached comprises a narrow neck (for example, element **271**), which has a width smaller than another width of the bond finger. In a still further embodiment, the semiconductor package can further comprise a dimple (for example, element **291**) in a major surface of the bond finger, at least a portion of the solder portion disposed within the dimple. In another embodiment, the dimple can be in an upper major surface of the bond finger adjacent the semiconductor chip. In a further embodiment, the semiconductor package can have a bump-to-lead ratio of about 2 or more. In a still further embodiment, the semiconductor package can comprise a micro lead frame package (for example, element **200**).

From all of the foregoing, one skilled in the art can determine that according to a further embodiment, an electronic package structure (for example, element **300**, **400**, **500**, **600**) comprises a lead (for example, element **20**) having a first width (for example, element **203**). An electronic chip (for example, element **101**) having a conductive bump (for example, element **301**) on a major surface, wherein the conductive bump has a second width (for example, element **320**) greater than the first width, and wherein the conductive bump is attached to the lead, wherein a portion of the conductive bump extends to at least partially surround a side surface of the lead. A molding compound resin (for example, element **40**) seals the electronic chip, the conductive bump, and at least a portion of the lead.

In another embodiment, the lead further comprises a bond finger (for example, element **222**) having the first width, wherein the conductive bump is attached to the bond finger. In a further embodiment, side surfaces of the lead have concave portions (for example, element **231**). In a still further embodiment, the electronic package can further comprise a dimple (for example, element **291**) in a major surface of the lead, wherein a portion of the conductive bump is within the dimple. In another embodiment, the portion (for example, element **342**) of the conductive bump completely surrounds a portion of the lead. In a still further embodiment, the conductive bump comprises a conductive pillar (for example, element **321**) and a solder portion (for example, element **341**) on a tip of the conductive pillar, wherein the solder portion extends to at least partially cover sides surfaces the lead. In another embodiment, the lead further comprises a narrow neck portion (for example, element **291**), the narrow neck portion having the first width, and wherein the lead has a third width greater than the first width. In a further embodiment, the second width to first width ratio is about 2 or more.

From all of the foregoing, one skilled in the art can determine that according to a still further embodiment, a method for forming a semiconductor package (for example, element **300**, **400**, **500**, **600**) comprises providing a lead frame (for example, element **200**) having a lead (for example, element **201**), the lead having a first width (for example, element **203**. The method includes providing a semiconductor chip (for example, element **101**) having a conductive bump (for example, element **301**) on a major surface, the conductive bump having a second width (for example, element **320**) greater than the first width. The method includes attaching the conductive bump to the lead, wherein after the attaching step, a portion of the conductive bump extends to at least partially surround side surfaces of the lead. The method includes encapsulating (for example, element **40**) the semiconductor chip, the conductive bump, and at least portions of the lead.

In another embodiment, the step of providing the lead frame can include providing a lead having one or more of: a concave portion on a side surface of lead (for example, element **321**), a narrow neck portion (for example, element **271**), or a dimple (for example, element **291**) in an upper surface of the lead. In a further embodiment, providing the conductive bump can include providing a conductive pillar (for example, element **321**) having a solder portion (for example, element **341**, **342**) on an end surface of the conductive pillar. In still further embodiment, the second width to first width ratio is greater than or equal to about 2.

In view of all of the above, it is evident that a novel structure and method of making the structure are disclosed. Included, among other features, is an electronic package having a lead configured for attaching to an electronic chip, such as a semiconductor chip, in a flip chip or chip attach arrangement. In one embodiment, the lead is narrower than the conductive bump used to attach the electronic chip to the lead. The lead is configured to facilitate a strengthened solder joint. In one embodiment, the lead is configured to facilitate the flow of solder partially around side surfaces of the lead. In one embodiment, the side surfaces are configured to increase the surface area for solder attachment. In one embodiment, side surfaces of the lead have concave shaped portions. In another embodiment, the solder layer completely surrounds a portion of the lead. In a further embodiment, the lead is configured to have a narrow neck portion for attaching the conductive bump to lead. The narrow neck portion can be configured to facilitate the flow of solder partially or completely around the lead. In a further embodiment, a dimple is placed in a major surface of the lead to increase the surface area for forming the solder joint.

The foregoing embodiments provide, among other things, a stronger joining force for the joint between each lead and the solder of the conductive bump, even if the width of each lead is reduced and the size of the conductive pillar of the conductive bump is increased upon fabricating the semiconductor package using smaller lead frames, such as micro lead frames. More particularly, even if the width of each lead is reduced and the size of the conductive bump is increased to cope with the fine pitch for each lead and the increase in size of the copper pillar of the conductive bump, soldering is performed such that the solder surrounds at least portions the lead, thus providing an improved joining force for the solder joint of the conductive bump relative to each lead.

While the subject matter of the invention is described with specific preferred embodiments and example embodiments, the foregoing drawings and descriptions thereof depict only typical embodiments of the subject matter, and are not therefore to be considered limiting of its scope. It is evident that many alternatives and variations will be apparent to those skilled in the art. For example, the configurations of neck portion **271** and dimple **291** are illustrative only and other patterns, shapes, and configurations are possible for providing desired bond strengthening. Also, molding compound resin **40** can be formed by overmolding and saw-through techniques, formed by cavity molding and punch techniques, or formed by other techniques as known to those of ordinary skill in the art.

As the claims hereinafter reflect, inventive aspects may lie in fewer than all features of a single foregoing disclosed embodiment. Thus, the hereinafter expressed claims are hereby expressly incorporated into this Detailed Description of the Drawings, with each claim standing on its own as a separate embodiment of the invention. Furthermore, while some embodiments described herein include some but not other features included in other embodiments, combinations of features of different embodiments are meant to be within the scope of the invention, and form different embodiments, as would be understood by those skilled in the art.

We claim:

1. A semiconductor package comprising:

a plurality of leads, each lead having a bond finger;

a semiconductor chip having a plurality of conductive bumps, each conductive bump including a conductive pillar and a solder portion, each conductive bump attached to one of the bond fingers; and

a molding compound resin molded to seal the semiconductor chip, at least portions of the leads, and the conductive bump, wherein a width of the conductive pillar is larger than a width of each of the leads, and wherein the solder portion extends beyond an upper surface of the bond finger and at least partially surrounds a surface area of a portion of the bond finger.

2. The semiconductor package of claim **1**, wherein the solder portion completely surrounds the surface area of the portion of the bond finger.

3. The semiconductor package of claim **1**, wherein at least a portion of the surface area comprises a concave portion.

4. The semiconductor package of claim **1**, wherein each bond finger has concave portions on opposing side surfaces in cross-sectional view.

5. The semiconductor package of claim **4** further comprising a dimple in a major surface of the bond finger, wherein the dimple is disposed between the concave portions.

6. The semiconductor package of claim **1**, wherein a portion of the bond finger where the conductive bump is attached comprises a narrow neck, which has a width smaller than another width of the bond finger.

7. The semiconductor package of claim **1** further comprising a dimple in a major surface of the bond finger, at least a portion of the solder portion disposed within the dimple.

8. The semiconductor package of claim **7**, wherein the dimple is in an upper major surface of the bond finger adjacent the semiconductor chip.

9. The semiconductor package of claim **1**, wherein the semiconductor package has a bump-to-lead width ratio of about 2 or more.

10. The semiconductor package of claim **9**, wherein the semiconductor package comprises a micro lead frame package.

11. An electronic package structure comprising:

a lead having a first width;

an electronic chip having a conductive bump on a major surface, wherein the conductive bump has a second width greater than the first width, and wherein the conductive bump is attached to the lead, wherein a portion of the conductive bump extends to at least partially surround a side surface of the lead; and

a molding compound resin sealing the electronic chip, the conductive bump, and at least a portion of the lead.

12. The structure of claim **11**, wherein the lead further comprises a bond finger having the first width, wherein the conductive bump is attached to the bond finger.

13. The structure of claim **11**, wherein side surfaces of the lead have concave portions.

14. The structure of claim **11** further comprising a dimple in a major surface of the lead, wherein a portion of the conductive bump is within the dimple.

15. The structure of claim **11**, wherein the portion of the conductive bump completely surrounds a portion of the lead.

16. The structure of claim **11**, wherein the conductive bump comprises a conductive pillar and a solder portion on a tip of the conductive pillar, wherein the solder portion extends to at least partially cover sides surfaces of the lead.

17. The structure of claim **11**, wherein the lead further comprises a narrow neck portion, the narrow neck portion having the first width, and wherein the lead has a third width greater than the first width.

18. The structure of claim **11**, wherein the second width to first width ratio is 2 or more.

19. A method for forming a semiconductor package comprising:

providing a lead frame having a lead, the lead having a first width;

providing a semiconductor chip having a conductive bump on a major surface, the conductive bump having a second width greater than the first width;

attaching the conductive bump to the lead, wherein after attaching the attaching step, a portion of the conductive bump extends to at least partially surround side surfaces of the lead; and

encapsulating the semiconductor chip, the conductive bump, and at least portions of the lead.

20. The method of claim **19**, wherein:

providing the lead frame includes providing a lead having one or more of: a concave portion on a side surface of lead, a narrow neck portion, or a dimple in an upper surface of the lead;

providing the conductive bump comprises providing a conductive pillar having a solder portion on an end surface of the conductive pillar; and

the second width to first width ratio is greater than or equal to about 2.

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